WHAT IS CLAIMED IS:

1. A processor comprising:

a register configured to store a mask; and

an execution core coupled to the register, wherein the execution core is configured, in response to a system call instruction, to selectively update each flag of a plurality of flags responsive to a corresponding indication in the mask.

2. The processor as recited in claim 1 wherein the execution core is configured to update a first flag of the plurality of flags in response to the corresponding indication in the mask being in a first state and wherein the execution core is configured to retain a current state of the first flag in response to the corresponding indication in the mask being in a second state.

3. The processor as recited in claim 2 wherein the execution core is configured to update the first flag by clearing the first flag.

4. The processor as recited in claim 3 wherein the corresponding indication is a bit.

5. The processor as recited in claim 4 wherein the first state comprises the bit being set.

6. The processor as recited in claim 1 wherein the execution core is coupled to receive an indication of an operating mode of the processor, and wherein the execution core is configured to selectively update each flag in the plurality of flags in a first operating mode, and wherein the execution core is configured not to perform a selective update in a second operating mode.

7. The processor as recited in claim 6 wherein the execution core is configured to perform a predetermined update of the plurality of flags in the second operating mode.

8. The processor as recited in claim 1 further comprising a second register configured to store the plurality of flags, wherein the execution core is configured to store the updated plurality of flags in the second register in response to the system call instruction.

9. An apparatus comprising:

a storage location configured to store a mask; and

a processor coupled to the storage location, wherein the processor is configured, in response to a system call instruction, to selectively update each flag of a plurality of flags responsive to a corresponding indication in the mask.

10. The apparatus as recited in claim 9 wherein the processor is configured to update a first flag of the plurality of flags in response to the corresponding indication in the mask being in a first state and wherein the processor is configured to retain a current state of the first flag in response to the corresponding indication in the mask being in a second state.

11. The apparatus as recited in claim 10 wherein the processor is configured to update the first flag by clearing the first flag.

12. The apparatus as recited in claim 11 wherein the corresponding indication is a bit.

13. The apparatus as recited in claim 12 wherein the first state comprises the bit being set.

14. The apparatus as recited in claim 9 wherein the processor is configured to selectively update each flag in the plurality of flags in a first operating mode, and wherein the processor is configured not to perform a selective update in a second operating mode.

15. The apparatus as recited in claim 14 wherein the processor is configured to perform a predetermined update of the plurality of flags in the second operating mode.

16. The apparatus as recited in claim 9 further comprising a second storage location configured to store the plurality of flags, wherein the processor is configured to store the updated plurality of flags in the second storage location in response to the system call instruction.

17. A method comprising processing a system call instruction, the processing including selectively updating each flag of a plurality of flags responsive to a corresponding indication in a mask.

18. The method as recited in claim 17 wherein the selectively updating comprises:

updating a first flag of the plurality of flags in response to a first state of the corresponding indication; and

retaining a current state of the first flag in response to a second state of the corresponding indication.

19. The method as recited in claim 18 wherein the updating the first flag comprises clearing the first flag.

20. The method as recited in claim 17 wherein the selectively updating is performed in a first operating mode, and wherein the selectively updating is not performed in a second

operating mode.

21. The method as recited in claim 20 further comprising performing a fixed update of the plurality of flags in the second operating mode.

22. A processor comprising:

a register configured to store a value; and

an execution core coupled to the register, wherein the execution core is configured, in response to a system call instruction, to selectively update each flag of a plurality of flags responsive to the value in the register.